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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/024,724

12/21/2001

Michael D. Haines

219.40853X00

5908

7590

03/02/2004

Kenyon & Kenyon
1500 K. Street N.W.
Suite 700
Washington, DC 20005

EXAMINER

WILLIAMS, ALEXANDER O

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/024,724

Applicant(s)

HAINES, MICHAEL D.

Examiner

Alexander O Williams

Art Unit

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AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 October 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) 28 and 29 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 6.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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Serial Number: 10/024724 Attorney's Docket #: 219.40853X00

Filing Date: 12/21/01;

Applicant: Haines

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 28) in Paper # 14, filed 10/21/03, has been acknowledged.

This application contains claims 29 and 30 drawn to an invention non-elected with traverse in Paper No. 14.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claims 11, 20 and 27 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 11, 20 and 27, it is unclear and confusing to the structure claimed by the language of "wherein the gasket has a shielding effectiveness to protect the die from at least 4 kV of electrostatic discharge pulse at a system level in which the electronic package is to be used."

Any of claims 11, 20 and 27 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 22, 24 and 26 to 28, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Morris (U.S. Patent # 6,507,101 B1).

22. Morris (figures 1A to 4B) specifically figure 2 show an electronic package with protection from electrostatic discharge events comprising: a substrate **210**; a semiconductor die **212** mounted on the substrate; a heat sink **206** in heat conducting relation with the semiconductor die on a side of the semiconductor die opposite the substrate; and a gasket of a lossy material **202** on the substrate surrounding the semiconductor die to protect the die from electrostatic discharge pulses.

24. The electronic package according to claim 22, Morris show wherein the lossy material of the gasket is a static dissipative material having, a volume resistivity of greater than 10¹² ohm cm.

26. Morris show wherein the gasket **22** has a hole therein the size of the die through which the die protrudes.

27. Morris show wherein the gasket has a shielding effectiveness to protect the die from at least 4 kV of electrostatic discharge pulse at a system level in which the electronic package.

28. Morris show wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz.

Claims 1, 3 to 8, 11, 12, 22 to 24, 27 and 28, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Barker, III et al. (U.S. Patent # 5,175,613).

1. Barker, III et al. (figures 1 and 2) specifically figure 2 show an assembly for packaging and cooling a semiconductor die comprising: a substrate **12**; a semiconductor die **24** mounted on the substrate; a thermal spreader **52** in heat conducting relation with the semiconductor die on a side of the die opposite the substrate; and a gasket of a lossy material **26** on the substrate surrounding the die to protect the die from electrostatic discharge pulses.
3. The assembly according to claim 1, Barker, III et al. further comprising a heat sink **14** in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the die.
4. The assembly according to claim 1, Barker, III et al. show wherein the semiconductor die is a microprocessor.
5. The assembly according to claim 1, Barker, III et al. show wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.
6. The assembly according to claim 5, Barker, III et al. show wherein the volume resistivity of the static dissipative material is less than 10^9 ohm cm.
7. The assembly according to claim 1, Barker, III et al. show wherein the gasket is bonded to the substrate with an adhesive **25**.
8. The assembly according to claim 7, Barker, III et al. show wherein the adhesive is conductive.
11. The assembly according to claim 1, Barker, III et al. show wherein the gasket has a shielding effectiveness to protect the die from at least 4 kV of electrostatic discharge pulse at a system level in which the assembly is to be used.
12. The assembly according to claim 1, Barker, III et al. show wherein the gasket material has a shielding effectiveness of greater than 45 dB tip to 3 GHz in frequency.
22. Barker, III et al. (figures 1 and 2) specifically figure 2 show an electronic package with protection from electrostatic discharge events comprising: a substrate **12**; a semiconductor die **24** mounted on the substrate; a heat sink **14** in heat conducting relation with the semiconductor die on a side of the semiconductor die opposite the substrate; and a gasket of a lossy material **26** on the substrate surrounding the semiconductor die to protect the die from electrostatic discharge pulses.

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23. The electronic package according to claim 22, Barker, III et al. show further comprising a thermal spreader located intermediate the semiconductor die and the heat sink to thermally couple the die and heat sink.

24. The electronic package according to claim 22, Barker, III et al. show wherein the lossy material of the gasket is a static dissipative material having, a volume resistivity of greater than 10^2 ohm cm.

27. Barker, III et al. show wherein the gasket has a shielding effectiveness to protect the die from at least 4 kV of electrostatic discharge pulse at a system level in which the electronic package.

28. Barker, III et al. show wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz.

Claims 1 to 8, 10 to 17, 19 to 21 and 23, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris (U.S. Patent # 6,507,101 B1) in view of Alcoe et al. (U.S. Patent Application Publication # 2003/0025180 A1).

1. Morris (figures 1A to 4B) specifically figure 2 show an assembly for packaging and cooling a semiconductor die comprising: a substrate **210**; a semiconductor die **212** mounted on the substrate; and a gasket of a lossy material **202** on the substrate surrounding the die to protect the die from electrostatic discharge pulses. Morris fails to explicitly show a thermal spreader in heat conducting relation with the semiconductor die on a side of the die opposite the substrate.

Alcoe et al. is cited for showing an EMI shielding for semiconductor chip carriers. Specifically, Alcoe et al. (figures 1 to 3) specifically figure 2 discloses a thermal spreader (**unlabeled electrically-conductive material between the heat sink 48 and chip 42 and substrate 40**) in heat conducting relation with the semiconductor die on a side of the die opposite the substrate (**see page 3, paragraph [0040]**) for the purpose of producing an EMI shield for the structure.

2. The assembly according to claim 1, the combination with Alcoe et al. showing wherein the thermal spreader extends beyond the outer peripheral edge of the die and overhangs an adjacent edge of the gasket **52**.

3. The assembly according to claim 1, the combination with Alcoe et al. further comprising a heat sink **48** in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the die **42**.

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4. The assembly according to claim 1, either show wherein the semiconductor die is a microprocessor.
5. The assembly according to claim 1, either show wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.
6. The assembly according to claim 5, either show wherein the volume resistivity of the static dissipative material is less than 10^9 ohm cm.
7. The assembly according to claim 1, the combination with Alcoe et al. showing wherein the gasket is bonded to the substrate with an adhesive **64** (see figure 3).
8. The assembly according to claim 7, the combination with Alcoe et al. showing wherein the adhesive is conductive.
10. The assembly according to claim 1, the combination with Morris show wherein the gasket **204** has a hole therein the size of the die through which the die protrudes.
11. The assembly according to claim 1, either reference show wherein the gasket has a shielding effectiveness to protect the die from at least 4 kV of electrostatic discharge pulse at a system level in which the assembly is to be used.
12. The assembly according to claim 1, either reference show wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz in frequency.
13. Morris (figures 1A to 4B) specifically figure 2 show an apparatus for increasing the immunity of a microprocessor form electrostatic discharge events comprising: a substrate **210**; a microprocessor **212** mounted on the substrate; a heat sink **206** in heat conducting relation on a side opposite the microprocessor; a gasket of a lossy material **202** on the substrate surrounding the microprocessor to protect the microprocessor from electrostatic discharge pulses; and a thermal spreader in heat conducting relation with the microprocessor on a side of the microprocessor opposite the substrate; a heat sink **206** in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the microprocessor; wherein the thermal spreader extends beyond the outer peripheral edge of the microprocessor and overhangs an adjacent edge of the gasket.

Alcoe et al. is cited for showing an EMI shielding for semiconductor chip carriers. Specifically, Alcoe et al. (figures 1 to 3) specifically figure 2 discloses a thermal spreader (**unlabeled electrically-conductive material between the heat sink 48 and chip 42 and substrate 40**) in heat conducting relation with the microprocessor on a side of the microprocessor opposite the substrate; a heat sink **48** in heat conducting

relation with the thermal spreader on a side of the thermal spreader opposite the microprocessor; wherein the thermal spreader extends beyond the outer peripheral edge of the microprocessor and overhangs an adjacent edge of the gasket (**see page 3, paragraph [0040]**) for the purpose of producing an EMI shield for the structure.

14. The apparatus according to claim 13, either reference show wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.

15. The apparatus according to claim 14, either reference show wherein the volume resistivity of the static dissipative material is less than 10^9 ohn cm.

16. The apparatus according to claim 13, the combination with Alcoe et al. showing wherein the gasket is bonded to the substrate with an adhesive **64** (see figure 3).

17. The apparatus according to claim 13, the combination with Morris showing wherein the gasket **202** is the size of the substrate.

19. The apparatus according to claim 13, the combination with Morris showing wherein the gasket has a hole therein the size of the microprocessor through which the microprocessor protrudes.

20. The apparatus according to claim 13, the combination with Morris showing wherein tile gasket has a shielding effectiveness to protect the microprocessor from at least 4 kV of electrostatic discharge pulse at a system level In which the apparatus is to be used.

21. The apparatus according to claim 13, the combination with Morris showing wherein. tile gasket material has a shielding effectiveness of greater than 45 dB tip to 3 GNz in frequency.

23. The electronic package according to claim 22, the combination with Alcoe et al. further comprising a thermal spreader located intermediate the semiconductor die and the heat sink to thermally couple the die and heat sink.

Therefore, it would have been obvious to one of ordinary skill in the art to use Alcoe et al.'s thermal spreader to modify Morris chip to heat sink connection for the purpose of producing an EMI shield for the structure.

Claims 9 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris (U.S. Patent # 6,507,101 B1) in view of Alcoe et al. (U.S. Patent Application Publication # 2003/0025180 A1) and further in view of Abe et al. (U. S. Patent # 5,749,586).

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Morris and Alcoe et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the gasket is formed of expanded polytetrafluorethylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

Abe et al. is cited for showing a gasket for sanitary piping. Specifically, Abe et al. (figures 1 to 3) specifically figure 1 discloses a gasket 1 is formed of expanded polytetrafluorethylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm for the purpose of recovering the sealing function by repeated retightening.

Therefore, it would have been obvious to one of ordinary skill in the art to use Abe et al.'s polytetrafluorethylene gasket to modify Morris/Alcoe et al.'s gasket for the purpose of recovering the sealing function by repeated retightening.

Claims 9 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Barker, III et al. (U.S. Patent # 5,175,613) in view of Abe et al. (U. S. Patent # 5,749,586).

Barker, III et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the gasket is formed of expanded polytetrafluorethylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

Abe et al. is cited for showing a gasket for sanitary piping. Specifically, Abe et al. (figures 1 to 3) specifically figure 1 discloses a gasket 1 is formed of expanded polytetrafluorethylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm for the purpose of recovering the sealing function by repeated retightening.

Therefore, it would have been obvious to one of ordinary skill in the art to use Abe et al.'s polytetrafluorethylene gasket to modify Barker III, et al.'s gasket for the purpose of recovering the sealing function by repeated retightening.

Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris (U.S. Patent # 6,507,101 B1) in view of Abe et al. (U. S. Patent # 5,749,586).

Morris show the features of the claimed invention as detailed above, but fail to explicitly show wherein the gasket is formed of expanded polytetrafluorethylene material

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filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

Abe et al. is cited for showing a gasket for sanitary piping. Specifically, Abe et al. (figures 1 to 3) specifically figure 1 discloses a gasket 1 is formed of expanded polytetrafluorethylene material filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm for the purpose of recovering the sealing function by repeated retightening.

Therefore, it would have been obvious to one of ordinary skill in the art to use Abe et al.'s polytetrafluorethylene gasket to modify Morris gasket for the purpose of recovering the sealing function by repeated retightening.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/659,660,706,700,701,712,713,177,675,676,721,790, 921 361/715,704,719,818	2/23/04
Other Documentation: foreign patents and literature in 257/659,660,706,700,701,712,713,177,675,676,721,790, 921 361/715,704,719,818	2/23/04
Electronic data base(s): U.S. Patents EAST	2/23/004


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
2/23/04

A handwritten signature in black ink, appearing to read 'Alexander Williams', with a stylized, sweeping flourish extending from the end of the signature.

Alexander Williams
Primary Examiner